



## AND-TFT-5VX

### 640 x 480 Pixels

### LCD Color Monitor

The AND-TFT-5VX is a compact full color TFT LCD module, whose driving board is capable of converting composite video signals to the proper interface of LCD panel and is suitable for computer peripheral, industrial meter, image communication and multi media.

This device consists of an amorphous silicon panel with back-light, incorporating a TFT-array that has 640 x 480 pixels on a 5 inch diagonal screen, with pixel in stripe configuration, 262,144 display colors and a TTL transmission interface.

#### Features

• RoHS Compliant

- VGA (640 x 480 pixels) resolution
- Amorphous silicon TFT LCD panel with back-lit unit
- Pixel in stripe configuration
- Light weight and slim
- Displays 262,144 colors
- Optimum Viewing Direction: 3 o'clock
- Portrait mode
- TTL transmission interface

Product specifications contained herein may be changed without prior notice. It is therefore advisable to contact Purdy Electronics before proceeding with the design of equipment incorporating this product.

#### Mechanical Characteristics

Parameter	Specification	Unit
Screen Size	5.0 (diagonal)	inch
Display Format	640 (H) x (R, G, B) x 480(V)	dot
Display Colors	262,144	
Active Area	74.88 (H)x101.76(V)	mm
Pixel Pitch	0.156(H)x0.159(V)	mm
Pixel Configuration	Stripe	
Outline Dimension	91.4(H)x119.3(V)x7.9(D)	mm
Weight	120±10	g
Back-light	CCFL, 1 tube	
Display Mode	Normally white	

#### Recommended Driving Condition for Back Light

Ta=25°C

Parameter	Symbol	Specifications			Unit	Remark
		Min.	Typ.	Max.		
Lamp Voltage	V <sub>L</sub>	390	410	430	V	I <sub>L</sub> =6mA
Lamp Current	I <sub>L</sub>	4.0	6.0	8.0	mA	Note 1
Lamp Frequency	P <sub>L</sub>	30	45	60	KHZ	Note 2
Starting Voltage (25°C) (Reference Value)	V <sub>s</sub>	—	—	640	Vrms	Note 3
Starting Voltage (0°C) (Reference Value)	V <sub>s</sub>	—	—	740	Vrms	Note 3

Note 1 : In order to satisfy the quality of B/L, no matter what inverter is used, the output lamp current must be between Min. and Max. to avoid the abnormal display image caused by B/L.

Note 2 : The waveform of lamp driving voltage should be as close to a perfect sine wave as possible.

Note 3 : The "Max of starting voltage" means the minimum voltage of inverter turns on the CCFL and it should be applied to the lamp for more than 1 second to start up. Otherwise the lamp may not be turned on.

**Power Consumption**

Parameter		Symbol	Conditions	Specifications			Remark
				Typ.	Max.	Unit	
Supply Current for Gate Driver	Hi level	$I_{GG}$	$V_{GG} = +15.4V$	0.090	0.100	mA	
Supply Current for Gate Driver	Low level	$I_{EE}$	$V_{EE} = -5.5V$	0.103	0.110	mA	
Supply Current for Source Driver(Digital)		$I_{DD1}$	$V_{DD1} = +3.3V$	4.7	5.0	mA	
Supply Current for Source Driver (Analog)		$I_{DD2}$	$V_{DD2} = +7.7V$	17	20	mA	
Supply Current for Gate Driver (Digital)		$I_{CC}$	$V_{CC} = +3.3V$	0.009	0.010	mA	
LCD Panel Power Consumption			-	146.5	155.0	mW	Note 1
Back Light Lamp Power Consumption			-	2.46	-	W	Note 2

Note 1: The power consumption for backlight is not included

Note 2: Backlight lamp power consumption is calculated by  $I_L \times V_L$ .

**Recommended Operating Conditions**
 $V_{SS1} = V_{SS2} = GND = 0V, T_a = 25^\circ C$ 

Item	Symbol	Specifications			Unit	Remark
		Min.	Typ.	Max.		
Supply Voltage for Source Driver	$V_{DD1}$	2.3	3.3	3.6	V	
	$V_{DD2}$	6.5	7.7	13.5		
Supply Voltage for Gate Driver	$V_{GG}$	14.4	15.4	16.4	V	
	$V_{EE}$	-6.0	-5.5	-5.0		
	$V_{CC}$	2.3	3.3	5.5		
$V_{oom}$ Voltage	$V_{ccm}$	-	2.6	-	V	
Digital Input Voltage	$V_{IH}$	$0.7 V_{CC}$	-	$V_{CC}$	V	
	$V_{IL}$	0	-	$0.3 V_{CC}$		

**Backlight Driving** - Connector type: JST BHSR-02VS-1, 2 Pins, Pitch: 4 mm

Pin No	Symbol	Description	Remark
1	VL1	Input terminal (Hi voltage side)	Wire color : Pink
2	VL2	Input Terminal (Low voltage side)	Wire color : White Note 1

Note 1: Low voltage side of backlight inverter connects with ground of inverter circuits.

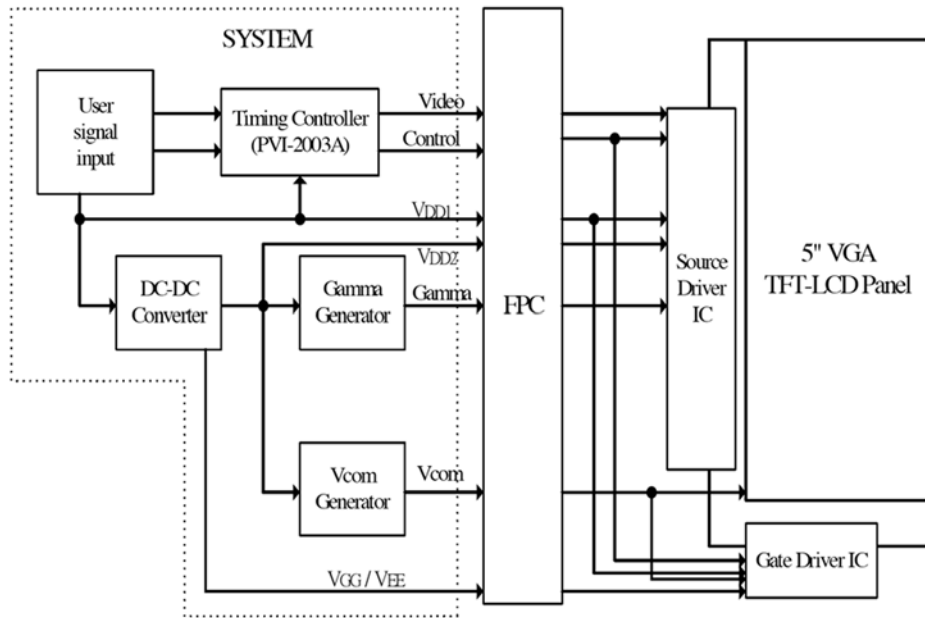
**Absolute Maximum Ratings:**
 $V_{SS1} = V_{SS2} = GND = 0V, T_a = 25^\circ C$ 

Parameters	Symbol	Min.	Max.	Unit	Remark
Supply Voltage	$V_{DD1}$	-0.5	5.0	V	
	$V_{CC}$	-0.3	6.0	V	
	$V_{DD2}$	-0.5	12.0	V	
	$V_{GG}$	-0.3	40.0	V	
	$V_{GG} - V_{EE}$	-0.3	40.0	V	
	$V_{EE}$	-20	0.3	V	

Optical Characteristics

Parameter	Symbol	Conditions	Specifications			Unit	Remarks
			Min.	Typ.	Max.		
Viewing Angle	Horizontal	$\theta = 21, 22$	CR $\geq 10$	55	60	deg	Note 1
	Vertical	$\theta = 12$ (3 o'clock)		55	60		
		$\theta = 11$ (9 o'clock)		40	45		
Contrast Ratio	CR		200	400	-	-	Note 2
Response Time	Rise	Tr	$\theta = 0^\circ$	-	15	ms	Note 3
	Fall	Tf		-	25		
Brightness	L	$\theta = 0^\circ/\psi = 0$	350	400	-	cd/m <sup>2</sup>	
Luminance Uniformity	U		70	75	-	%	Note 4
Lamp Life Time			50000	-	-	hr	At 6mA
White Chromaticity	x		0.28	0.31	0.34	-	
	y		0.34	0.37	0.40	-	
Cross Talk		$\theta = 0^\circ$	-	-	3.5	%	Note 5

Block Diagram



**Recommended Operating Conditions (Driving for Backlight)**
**Ta = 25°C**

Item	Symbol	Remark	Specifications			Unit
			Min.	Typ.	Max.	
Lamp Voltage	$V_L$	$I_L = 5 \text{ mA}$	432	480	528	Vrms
Lamp Current	$I_L$	–	4.5	5.0	5.5	mA
Lamp Frequency	$P_L$	Note 1	40	43	80	KHz
Kick-Off Voltage (25 °C)	$V_S$	Note 2	–	–	600	Vrms
Kick-Off Voltage (0 °C)	$V_S$		–	–	800	Vrms

Note 1: The wave form of lamp driving voltage should be as close to a perfect SIN wave as possible

Note 2: This value is not output voltage of inverter. The voltage of inverter must be larger than the starting voltage.

**Input / Output Terminals:**
**TFT-LCD Panel Driving**
**CN 1: FPC Down Connect, 30 pins, Pitch: 0.5 mm**

Pin #.	Symbol	I/O	Function	Remark
1	DIO1	I/O	Horizontal Start Pulse Signal Input or Output	Note 6
2	VSS1	I	Ground	
3	VDD1	I	Power Supply for Source	
4	CLK	I	Horizontal Shift Clock)	
5	VSS1	I	Ground	
6	R/L	I	RightLeft selection	Note 6
7	R0	I	Red Data (LSB)	
8	R1	I	Red Data	
9	R2	I	Red Data	
10	R3	I	Red Data	
11	R4	I	Red Data	
12	R5	I	Red Data (MSB)	
13	VSS1	I	Ground	
14	G0	I	Green Data (LSB)	
15	G1	I	Green Data	
16	G2	I	Green Data	
17	G3	I	Green Data	
18	G4	I	Green Data	
19	G5	I	Green Data (MSB)	
20	VSS1	I	Ground	
21	B0	I	Blue Data (LSB)	
22	B1	I	Blue Data	
23	B2	I	Blue Data	
24	B3	I	Blue Data	
25	B4	I	Blue Data	
26	B5	I	Blue Data (MSB)	
27	LD	I	Load output signal	Note 7
28	REV	I	Data invert control	Note 8
29	POL	I	Polarity	Note 9
30	DIO2	I/O	Horizontal Start Pulse Signal Input or Output	Note 6

**CN 2**

Pin #.	Symbol	I/O	Function	Remark
1	VSS2	I	Ground	
2	V1	I	Gamma Voltage 1	Note 10
3	V2	I	Gamma Voltage 2	Note 10
4	V3	I	Gamma Voltage 3	Note 10
5	V4	I	Gamma Voltage 4	Note 10
6	V5	I	Gamma Voltage 5	Note 10
7	V6	I	Gamma Voltage 6	Note 10
8	V7	I	Gamma Voltage 7	Note 10
9	VSS2	I	Ground	
10	V8	I	Gamma Voltage 8	Note 10
11	V9	I	Gamma Voltage 9	Note 10
12	V10	I	Gamma Voltage 10	Note 10
13	V11	I	Gamma Voltage 11	Note 10
14	V12	I	Gamma Voltage 12	Note 10
15	V13	I	Gamma Voltage 13	Note 10
16	V14	I	Gamma Voltage 14	Note 10
17	VSS2	I	Ground	
18	VDD2	I	Voltage for analog circuit	Note 10
19	VCOM	I	Common Voltage	
20	XON	I	NC	
21	OE	I	Output Enable	Note 5
22	U/D	I	Up/Down Selection	Note 3
23	CKV	I	Vertical Shift Cllock	Note 4
24	STVU	I/O	Vertical Shift Pulse Signal Input or Output	Note 3
25	STVD	I/O	Vertical Shift Pulse Signal Input or Output	Note 3
26	VGG	I	Gate On Voltage	Note 2
27	GND	I	Ground	
28	VCC	I	Voltage for logic circuit	
29	GND	I	Ground	
30	VEE	I	Gate Off Voltage	Note 1

Note 1: Gate off voltage,  $V_{EE} = -5.5V$ .

Note 2: Gate on voltage,  $V_{GG} = 15.4V$ .

Note 3: Select up or down shift (**see Table 1**)

Note 4: Gate driver shift clock

Note 5: When OE is connected to high "1", the driver outputs are disabled (Gate output= $V_{EE}$ ). Under this condition, the operation of registers will not be affected.

Note 6: Select left or right shift (**see Table 2**)

Note 7: Latch the polarity of outputs and switch the new data to outputs. At the rising edge (LD), latch the "POL" signal to control the polarity of the outputs.

Note 8: Control whether the Data RO~G5 are inverted or not. (PVI suggests connecting to GND) When "REV=1" these data will be inverted. EX: "00" to "3F", "07" to "38", "15" to "2A"

Note 9: Polarity selector for dot-inversion control. Available at the rising edge of LD. When POL=1: Even outputs range from V1~V7, and Odd outputs range from V8~V14, and Odd outputs range from V1~V7.

Note 10: VDD2 = 7.7V (Typical Application Circuit (when V1=7.7V))

**Table 1**

U / D	STVU	STVD	Shift
1	Hi-Z	Input	Down to Up
0	Input	Hi-Z	Up to Down

**Table 2**

R / L	DIO2	DIO2	Shift
1	Input	Hi-Z	Left to Right
0	Hi-Z	Input	Right to Left

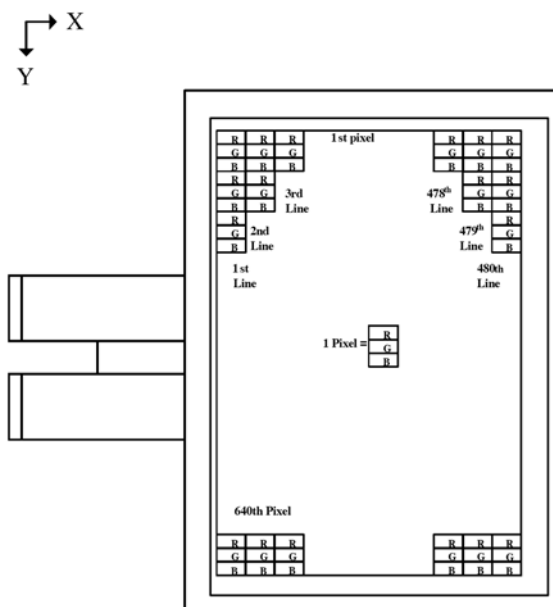
**Interface Timing**

 AC Electrical Characteristics ( $V_{CC}=V_{DD1}=3.3V$ ,  $V_{DD2}=9.5V$ ,  $GND=V_{SS1}=V_{SS2}=0V$ ,  $T_a=25^{\circ}C$ )

Parameter	Symbol	Min.	Typ.	Max.	Unit
CLK Frequency	Fclk	–	25	40	MHz
CLK Pulse Width	Tcw	25	40	–	ns
Data Sett-up Time	Tsu	4	–	–	ns
Data Hold Time	Thd	2	–	–	ns
Propagation Delay of DIO2/1	Tphl	6	10	15	ns
Time That the Last Data to LD	Tld	1	–	–	Tcw
Pulse width of LD	Twld	2	–	–	Tcw
Time That LD tp DIO1/2	Tlds	5	–	–	Tcw
POL Set-up Time	Tpsu	6	–	–	ns
POL Hold Time	Tphd	6	–	–	ns
OE Pulse Width	T <sub>OE</sub> V	1	–	–	μs
CKV Pulse Width	T <sub>CKV</sub>	500	–	–	ns
STV Set-up Time	T <sub>SUV</sub>	400	–	–	ns
STV Hold Time	T <sub>H</sub> DV	400	–	–	ns
Horizontal Display Period	T <sub>HDP</sub>	–	640	–	Tcw
Horizontal Period Timing Range	T <sub>HP</sub>	–	800	–	Tcw
Horizontal Lines Per Field	T <sub>V</sub>	520	525	640	T <sub>HP</sub>
Vertical Display Timing Range	T <sub>DV</sub>	–	480	–	T <sub>HP</sub>

**Pixel arrangement**

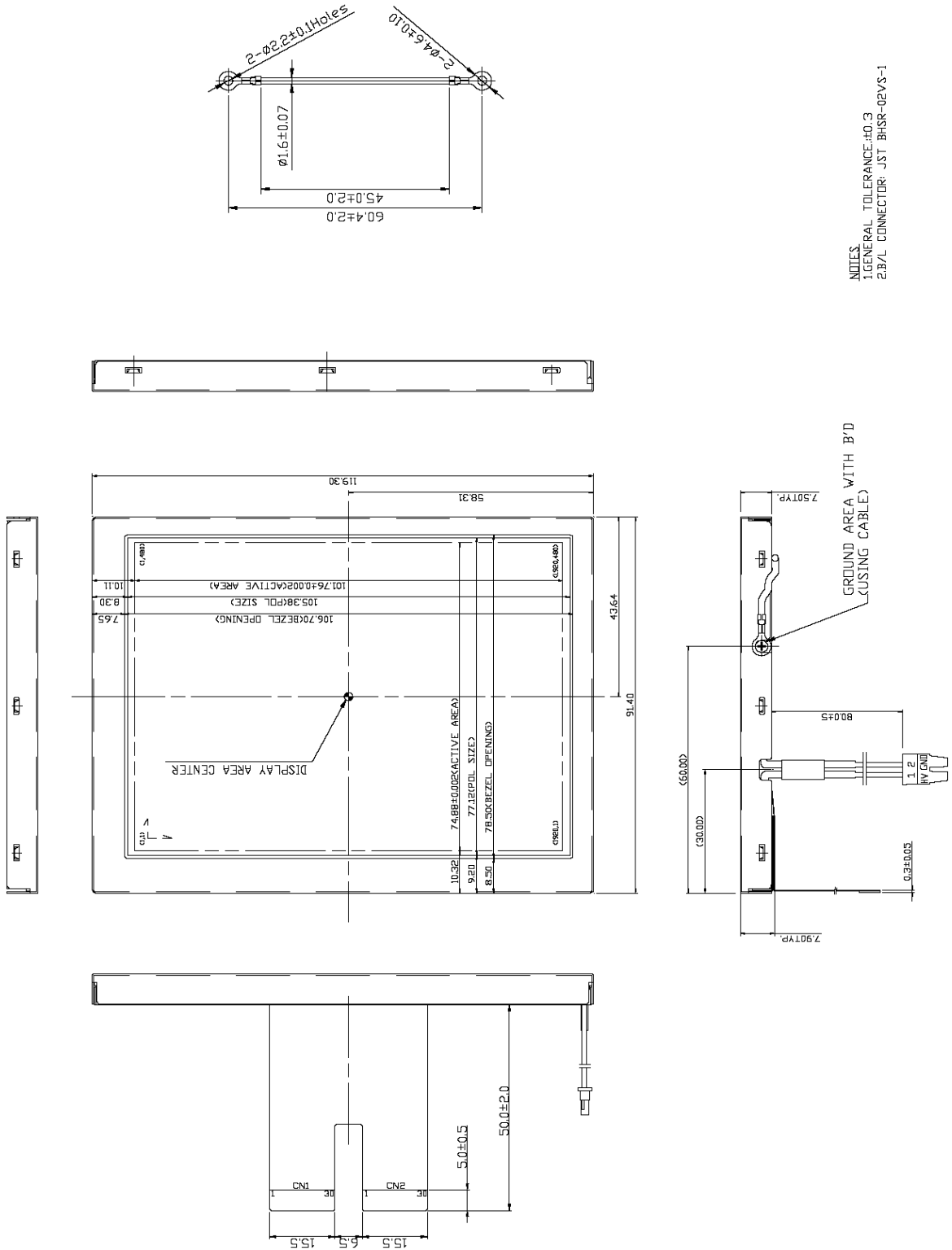
LCD module pixel arrangement is the stripe.


**Reliability Test**

No	Test Item	Test Condition	Remark
1	High Temperature Storage Test	Ta = +80°C, 240 hrs	
2	Low Temperature Storage Test	Ta = -30°C, hrs	
3	High Temperature Operation Test	Ta = +70°C, 240 hrs	
4	Low Temperature Operation Test	Ta = -20°C, 240 hrs	
5	High Temperature & High Humidity Operation Test	Ta = +60°C, 90%RH, 240 hrs (No Condensation)	
6	Thermal Cycling Test (non-operating)	-30°C to +80°C, 100 Cycles 30 min 30 min	
7	Vibration Test (non-operating)	Frequency : 10~55 Hz Amplitude : 1 mm Sweep Time : 11 min Test Period: 6 Cycles for each direction of X,Y,Z	
8	Shock Test (non-operating)	100G, 6ms Direction : ±X, ±Y, ±Z Cycle : 3 times	
9	Electrostatic Discharge Test (non-operating)	200pF, 0σ ±200V 1 time / each terminal	

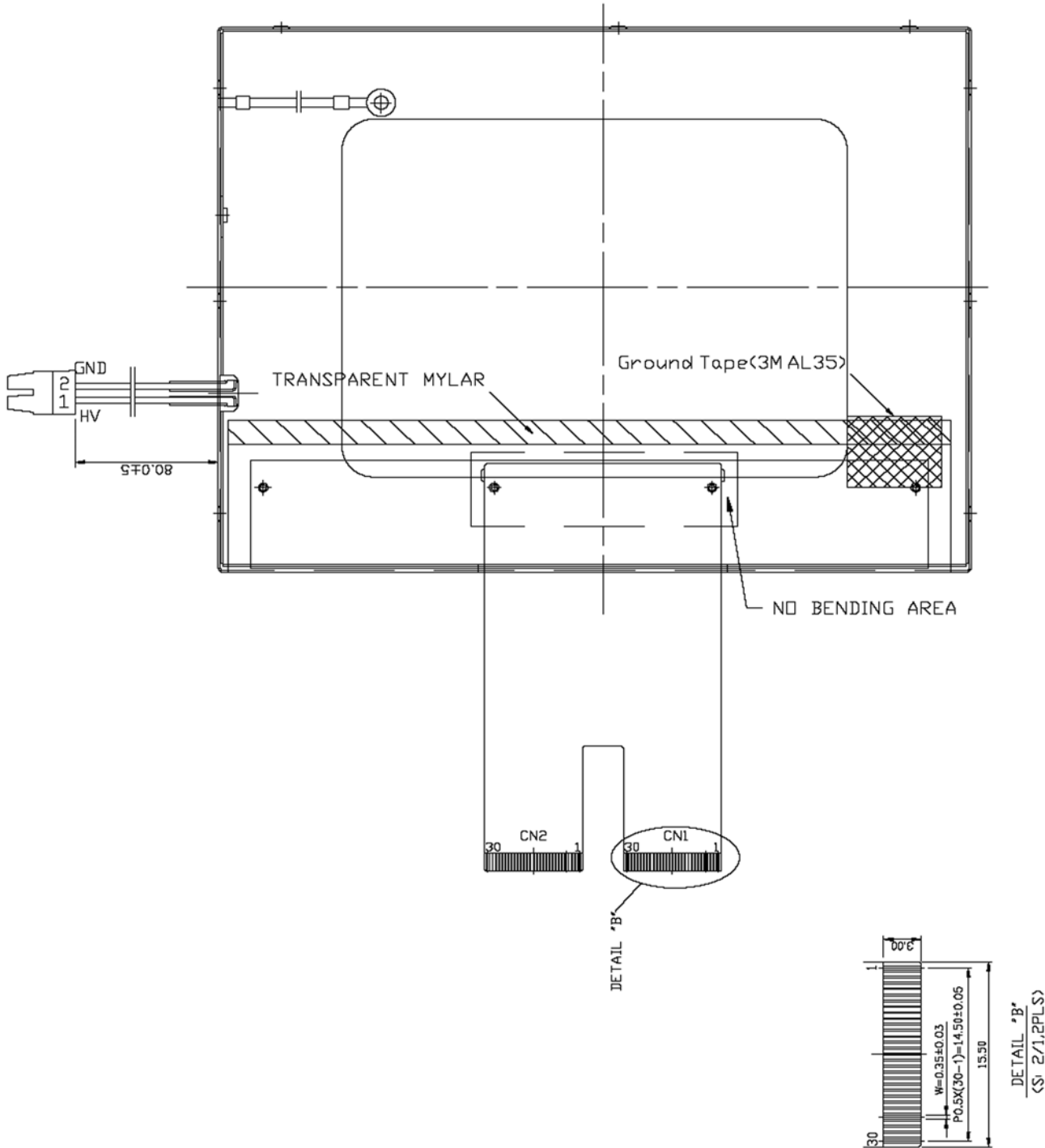
**Mechanical Drawing of TFT-LCD Module**

Outline Drawing : Front View (unit mm)



NOTES  
 1. GENERAL TOLERANCE: ±0.3  
 2. B/L CONNECTOR: JST BHSR-02V5-1

Outline drawing : Rear View (unit mm)





**Display Color and Gray Scale Reference**

Color		Input Color Data																	
		Red						Green						Blue					
		R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Basic Color	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Green (63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Blue (63)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale of Red	Red (00)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Dark ↑ ↓	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
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	Light	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	
Red (63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	
Gray Scale of Green	Green (00)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Dark ↑ ↓	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
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	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0	
Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	
Gray Scale of Blue	Blue (00)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Dark ↑ ↓	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
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	Light	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1
	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	
Blue (63)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	