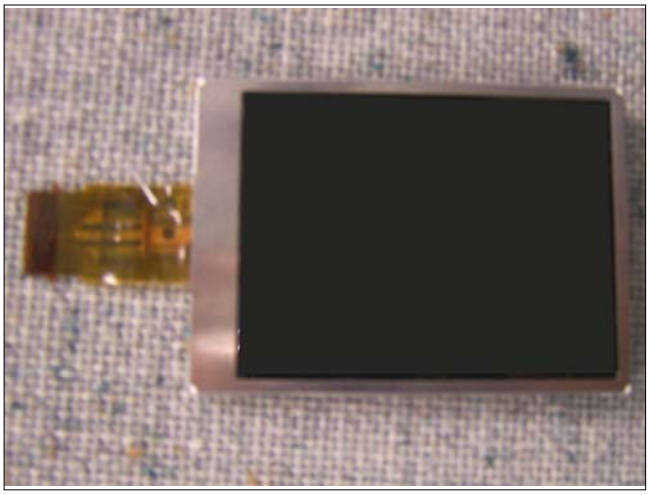


ANDpSi025TD-LED

320 x 240 Pixels
TFT LCD Color Monitor

The ANDpSI025TD-LED is a 2.5" active matrix color TFT LCD module, that is suitable for applications such as a portable television (NTSC), camcorder, digital camera applications and other electronic products which require high quality flat panel displays. LTPS (Low Temperature Poly Silicon) TFT technology is applied with vertical and horizontal drivers built on the panel. Both horizontal and vertical scan are reversible and controlled by the serial interface commands. The product is designed for the requirement of the green product, and the specification complies with Toppoly's "Green Product Chemical Substance Specification Standard Hand Book."

Features

- Long Life LED Backlight
- Active Matrix Color TFT LCD Module
- LTPS (Low Temperature Poly Silicon) TFT technology
- High Resolution: 320 x 240
- High Brightness
- Optimum Viewing Direction: 6 o'clock
- Up/Down and Left/Right Image Reversion
- Requires external chroma decoder to accept composite video card
- **RoHS compliant**

Mechanical Characteristics

Item	Specification	Unit
Screen Size	2.5 diagonal	inch
Display Type	Transmissive	–
Active Area	50.91 (W) x 38.16 (H)	mm
Pixel Count	960 (W) x 240 (H)	dot
Pixel Pitch	0.053 (W) x 0.159 (H)	mm
Color Arrangement	R.G.B. Delta	–
Color Numbers	16 million	–
Outline Dim.	61.7(W) x 44.5 (H) x 2.68* (D)	mm
Weight	15	g
Panel Surface Treatment	Hard Coating (3H)	–

* Exclude FPC and protrusions.

Absolute Maximum Rating (GND = 0V, Ta = 25°C)

Item	Symbol	Min.	Max.	Unit	Remark
Logic Power Supply Voltage	V_{CC}	-0.5	4.5	V	–
Input Signal Voltage	V_{IN1}	0	V_{CC}	V	VD, HD, DCLK, DIN[0:7], SDA, SCL, SCEN, SHDB, GRESTB
Backlight Forward Current	I_F	–	25	mA	–
Operating Temperature (note 1)	Topr	-10	+60	°C	–
Storage Temperature	Tstg	-30	+80	°C	–

Product specifications contained herein may be changed without prior notice.
It is therefore advisable to contact Purdy Electronics before proceeding with the design of equipment incorporating this product.

Electrical Characteristics - Driving TFT LCD Panel

Item		Symbol	Specifications			Units	Remark
			Min.	Typ.	Max.		
Power Supply Voltage		V_{CC}	2.85	3.0	3.6	V	Note 1
Input Signal Voltage	Low Level	V_{IL}	GND	–	0.2x Vcc*	V	VD, HD, DCLK, DIN[0:7], SDA, SCL, SCEN, SHDB, GRESTB
	High Level	V_{IH}	0.8x Vcc*	–	Vcc*	V	
PWM Output Voltage		V_{PWM}	0	–	Vcc*	V	–
Feedback Voltage		V_{FB}	0.55	0.6	0.65	V	Note 2
Panel Power Consumption		W_P	–	50	60	mW	–

V_{CC}* - V_{CC} (TYP)
Note 1: The Vcc power is provided for overall panel module supply voltage.
Note 2: DC/DC feedback control voltage

(GND = 0V, Ta=25ºC)

Electrical Characteristics - Driving Backlight (Ta = 25ºC)

Item	Symbol	Specifications			Unit	Remarks
		Min.	Typ.	Max.		
Forward Current	I_F	–	23	25	mA	Note 1
Forward CurrentVoltage	V_F	–	7.2	8	V	
Backlight Power Consumption	W_{BL}	–	166	200	mW	

Note 1: Backlight driving circuit is recommended as the fix current circuit.

Optical Specifications

Item		Symbol	Conditions	Specifications			Unit
				Min.	Typ.	Max.	
Viewing Angle	Horizontal	θ		± 45	± 50	–	deg
	Vertical	θ (to 12 o'clock)	CR ≥ 10	10	15	–	
		θ (to 6 o'clock)		30	35	–	
Contrast Ratio		CR	At optimized viewing angle	100	120	–	
Response Time	Rise	Tr	θ = 0°	–	15	30	ms
	Fall	Tf	ϕ = 0°	–	25	50	
Transmission	Ratio	T	–	7.5	8.0	8.5	%
Uniformity		U	–	65	70	–	ms
Brightness		LUM	–	200	250	–	cd/m^2
White Chromaticity		X	θ = 0°	0.250	0.300	0.350	–
		Y		0.280	0.330	0.380	
		Tc		6650	6850	7050	
LED Life Time	+ 25°C	–	–	10,000	–	–	hr

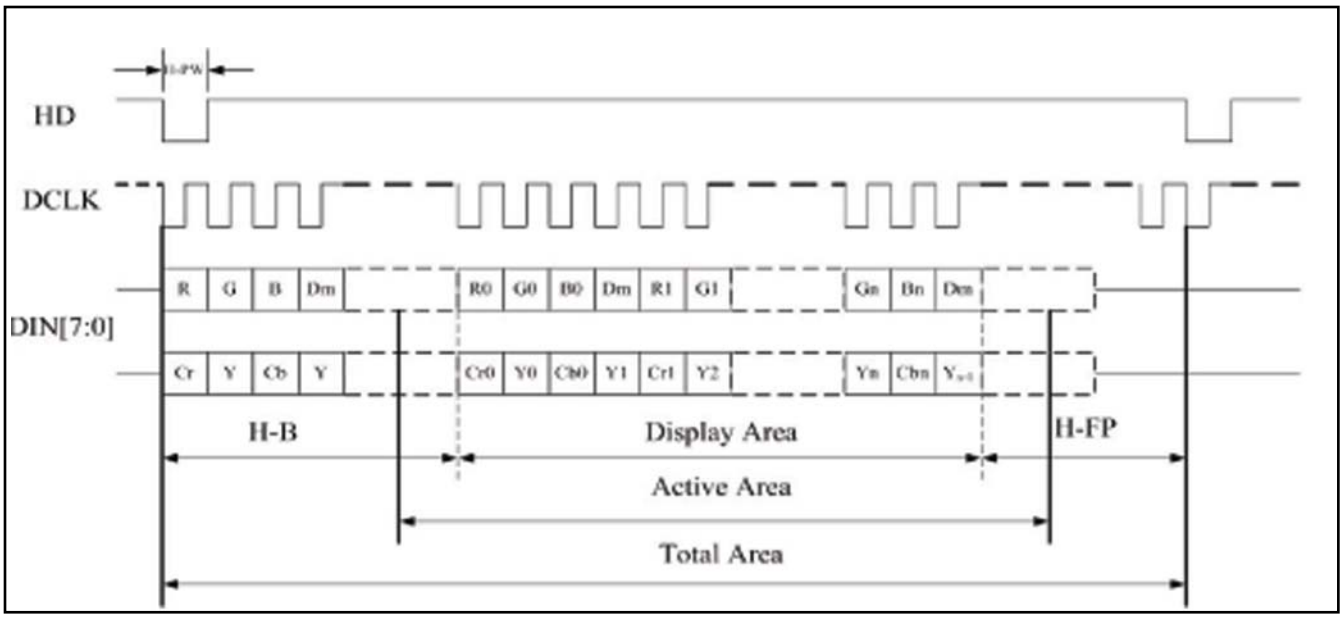
Note 1: CR= Luminance when LCD is White / Luminance when LCD is Black

Contrast Ratio is measured in optimum common electrode voltage.

Timing Characteristics - YUV Mode: ITUR601-NTSC

Item	Symbol	Min	Typ	Max	Unit
Dot Clock Frequency	DCLK	–	27	–	MHz
Horizontal Display Active	Display Area	–	1440	–	DCLK
Horizontal Total Time	Total Area	–	1716	–	DCLK
HSYNC Pulse Width	H-PW	–	1	–	DCLK
Horizontal Back Porch	H-B	–	240	–	DCLK
Horizontal Front Porch	H-FP	–	36	–	DCLK

Timing Chart - Serial RGB Dummy Mode and Serial YUV 4:2:2 Mode: Horizontal



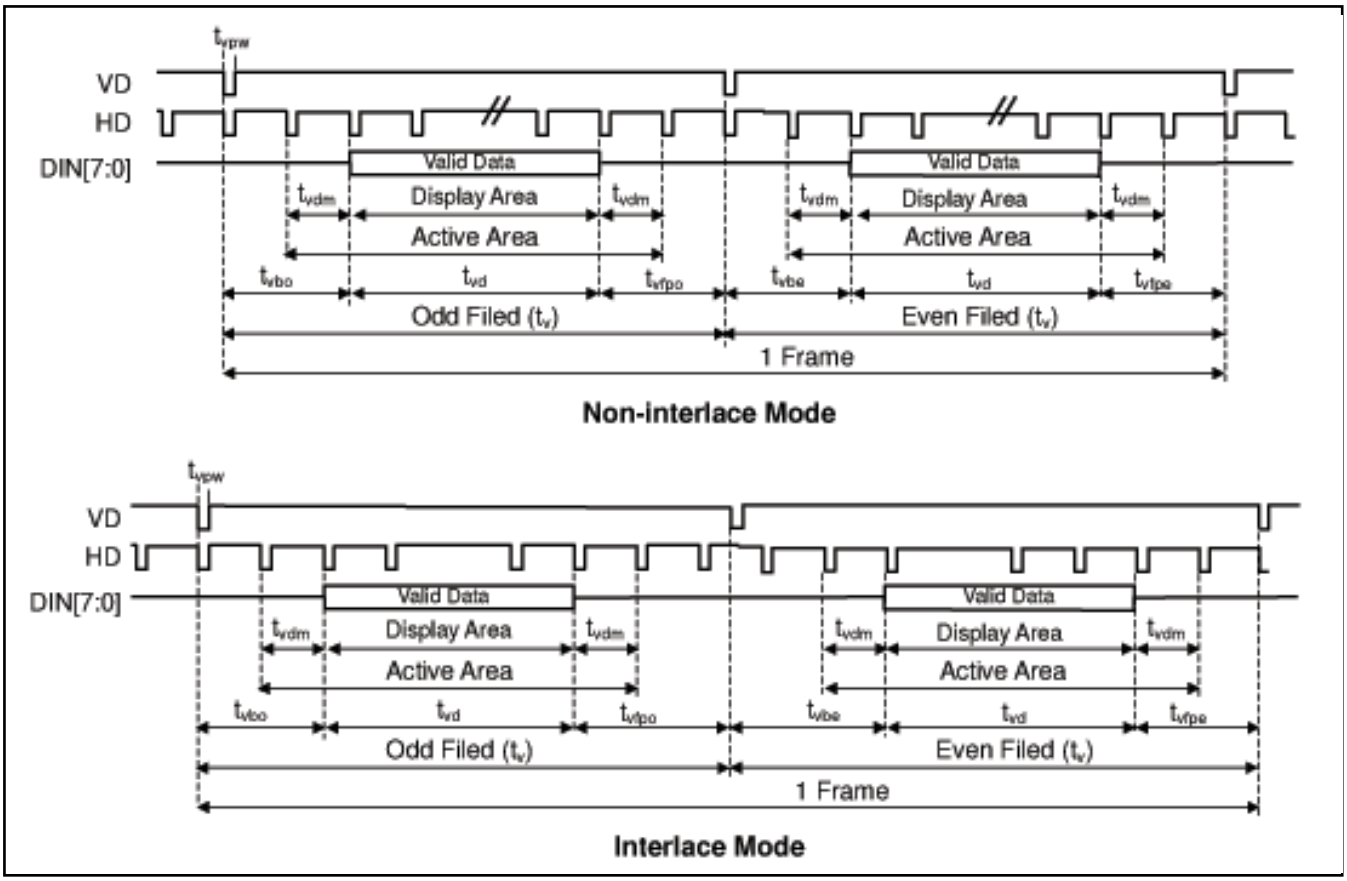
Timing Characteristics - YUV Mode: ITUR601-PAL

Item	Symbol	Min.	Typ.	Max.	Unit
Dot Clock Frequency	DCLK	–	27	–	MHz
Horizontal Display Active	Display Area	–	1440	–	DCLK
Horizontal Total Time	Total Area	–	1728	–	DCLK
HSYNC Pulse Width	H-PW	–	1	–	DCLK
Horizontal Back Porch	H-B	–	240	–	DCLK
Horizontal Front Porch	H-FP	–	48	–	DCLK

Timing Characteristics - Dummy Mode

Item		Symbol	Min.	Typ.	Max.	Unit
Dot Clock Frequency	QVGA	DCLK	–	25	–	MHz
	NTSC		–	24.54	–	
	PAL		–	24.38	–	
Horizontal Display Active		Display Area	–	1280	–	DCLK
Horizontal Total Time		Total Area	–	1560	–	DCLK
HSYNC Pulse Width		H-PW	–	1	–	DCLK
Horizontal Back Porch		H-B	–	240	–	DCLK
Horizontal Front Porch		H-FP	–	40	–	DCLK

Timing Chart - Serial RGB Dummy Mode and Serial YUV 4:2:2 Mode: Vertical



Timing Characteristics - Non-Interlace Mode: NTSC/QVGA

Item		Symbol	Min.	Typ.	Max.	Unit
Vertical Display Active		t_{VD}	–	240	–	Line
Vertical Total TIme		t_V	–	262	–	Line
VSYNC Pulse Width		t_{VPW}	1	1	–	DCLK
Vertical Back Porch	Odd Field	t_{VBO}	–	21	–	Line
	Even Field	t_{VBE}	–	21	–	Line
Vertical Front Porch	Odd Field	t_{VFPO}	–	1	–	Line
	Even Field	t_{VFPE}	–	1	–	Line
Vertical Dummy		t_{VDM}	–	0	–	Line

Timing Characteristics - Non-Interlace Mode: PAL

Item		Symbol	Min.	Typ.	Max.	Unit
Vertical Display Active		t_{VD}	–	288	–	Line
Vertical Total TIme		t_V	–	312	–	Line
VSYNC Pulse Width		t_{VPW}	1	1	–	DCLK
Vertical Back Porch	Odd Field	t_{VBO}	–	24	–	Line
	Even Field	t_{VBE}	–	24	–	Line
Vertical Front Porch	Odd Field	t_{VFPO}	–	0	–	Line
	Even Field	t_{VFPE}	–	0	–	Line
Vertical Dummy		t_{VDM}	–	0	–	Line

Timing Characteristics - Interlace Mode: NTSC/QVGA

Item		Symbol	Min.	Typ.	Max.	Unit
Vertical Display Active		t_{VD}	–	240	–	Line
Vertical Total TIme		t_V	–	262.5	–	Line
VSYNC Pulse Width		t_{VPW}	1	1	–	DCLK
Vertical Back Porch	Odd Field	t_{VBO}	–	21	–	Line
	Even Field	t_{VBE}	–	21.5	–	Line
Vertical Front Porch	Odd Field	t_{VFPO}	–	1.5	–	Line
	Even Field	t_{VFPE}	–	1	–	Line
Vertical Dummy		t_{VDM}	–	0	–	Line

Timing Characteristics - Interlace Mode: PAL

Item		Symbol	Min.	Typ.	Max.	Unit
Vertical Display Active		t_{VD}	–	288	–	Line
Vertical Total TIme		t_V	–	312.5	–	Line
VSYNC Pulse Width		t_{VPW}	1	1	–	DCLK
Vertical Back Porch	Odd Field	t_{VBO}	–	24	–	Line
	Even Field	t_{VBE}	–	24.5	–	Line
Vertical Front Porch	Odd Field	t_{VFPO}	–	0.5	–	Line
	Even Field	t_{VFPE}	–	0	–	Line
Vertical Dummy		t_{VDM}	–	0	–	Line

Optical Characteristics - Ta = 25ºC

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Remarks
Viewing Angles		θ 11	CR ≥ 10	30	40	–	Degree	Note 1
		θ 12		30	40	–		
		θ 21		15	20	–		
		θ 22		40	50	–		
Contrast Ratio		CR	θ = 0°	200	300	–	–	
Response Time	Rising	Tr		–	13	20	ms	
	Falling	Tf		–	22	30		
Luminance (I_F = 20 mA)		L		200	250	–	cd/m^2	
Chromaticity	White	x_W		0.26	0.31	0.36	–	
		y_W		0.28	0.33	0.38		

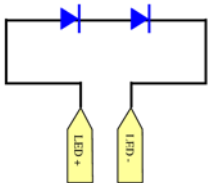
Note 1: Driving voltage: VCC = 3V, Ambient Temperature: Ta = 25ºC, Testing point:: measure in the display center point and the test angle θ = 0º, LED Current: I_F = 23 mA, Testing Facility: Environmental illumination: ≤ 1 Lux

Interface Pin Assignment - TFT LCD Panel

Pin No.	Symbol	Function	Input/Output	Remarks
1	CP3	Capacitor for charge pump	C	–
2	CP4	Capacitor for charge pump	C	–
3	CP5	Capacitor for charge pump	C	–
4	CP6	Capacitor for charge pump	C	–
5	CP7	Capacitor for charge pump	C	–
6	CP8	Capacitor for charge pump	C	–
7	NC	No connection	–	–
8	PCDL	Capacitor for pre-charge data signal low	C	–
9	PCDH	Capacitor for pre-charge data signal high	C	–
10	VCOML	Capacitor for VCOM low	C	–
11	VCOMH	Capacitor for CVOMhigh	C	–
12	AGND	Analog ground	–	–
13	PVDD	Regulation capacitor for charge pump	C	–
14	AVDD	Regulation capacitor for analog voltage	C	–
15	CP1	Capacitor for charge pump	C	–
16	CP2	Capacitor for charge pump	C	–
17	PWM	Power Transistor Gate Signal for the Boost Converter	O	–
18	FB	Main boost regulator feedback input	I	–
19	LED-	LED power: cathode	–	Note 1
20	LED+	LED power: anode	–	Note 1
21	NC	No connection	–	–
22	GND	Ground	–	–
23	VCC	Power Supply	–	–
24	VD	Vertical Sync Input	I	–
25	HD	Horizontal Sync Input	I	–
26	DCLK	Clock Signal, Latch Data Onto Line Latches at the Rising Edge	I	–
27	DIN0	Data Input	I	–
28	DIN1	Data Input	I	–
29	DIN2	Data Input	I	–
30	DIN3	Data Input	I	–
31	DIN4	Data Input	I	–
32	DIN5	Data Input	I	–
33	DIN6	Data Input	I	–
34	DIN7	Data Input	I	–
35	SDA	Serial Interface Data Line	I/O	–
36	SCL	Serial Interface Clock Line	I	–
37	SCEN	Serial Interface Chip Enable Line	I	–
38	SHDB	Sleep Mode Setting Pin	I	–
39	GRESTB	Global Reset Pin	I	–

(Recommended connector: JAE IL-FHJ-39S-HF-A1, HRS FH23-39S-0.3SHW(0.5), Molex SD54809-3957, IRISO 9671S39Y902)

Note 1: The figure to the right shows the connection of backlight LED.



Dimensional Outline